

October 28, 2020

NJG1162K64

Wideband Low Noise Amplifier

S-parameter Simulation Data

Standard Condition

Ver.0

- Touchstone file (s3p)
 - S3p file at $V_{DD}=3.3V$, $V_{CTL}=1.8V$: NJG1162_LNA.s3p (LNA mode)
 - S3p file at $V_{DD}=3.3V$, $V_{CTL}=0V$: NJG1162_BYPASS.s3p (Bypass mode)
- Simulation Circuit
- S-parameter Simulation Data
- Simulation Example

Written by Kenichi Nomura

Approved by Susumu Takagi

RFIC Design Section
RF Product Development Department
Technology Development Division

Nisshinbo Micro Devices Inc.



■ Touchstone file (s3p)

File Name :

NJG1162_LNA.s3p

- LNA mode

NJG1162_BYPASS.s3p

- Bypass mode

Simulation conditions :

$V_{DD}=3.3V$

$V_{CTL}=1.8V / 0V$ (LNA mode / Bypass mode)

$T_a=+25^{\circ}C$

$Z_s=Z_l=50\Omega$

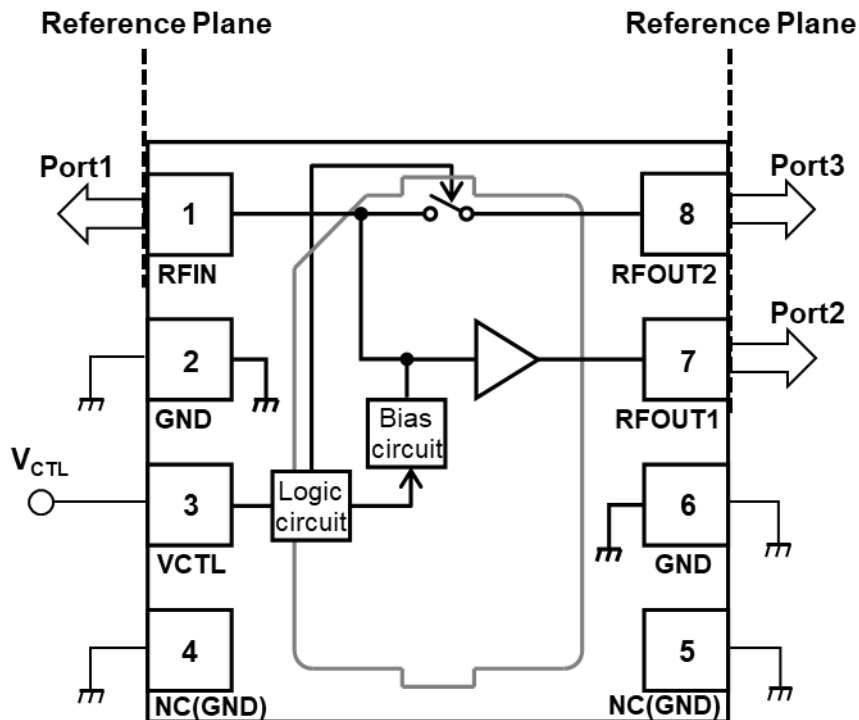
$f=10$ to $3000MHz$, $10MHz$ step

Port1 : RFIN

Port2 : RFOUT1

Port3 : RFOUT2

■ Simulation Circuit

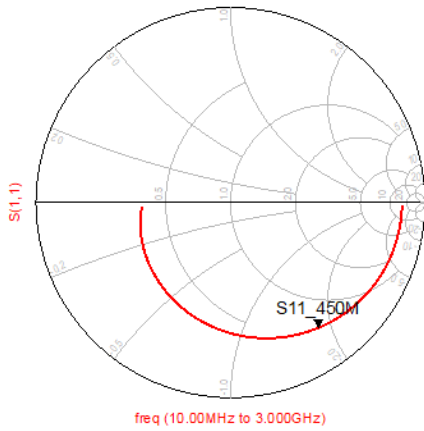


Note : Power supply voltage V_{DD} is applied from Port2 using the ideal bias T (DC feed L and DC blocking C).

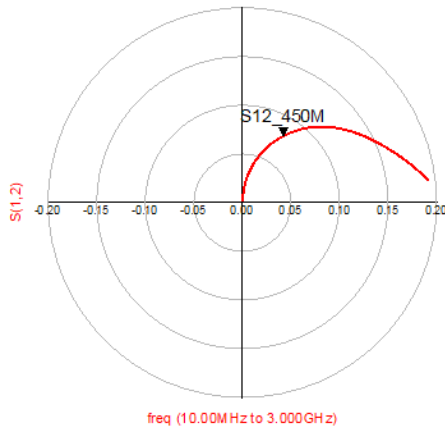


■ S-parameter Simulation Data (LNA mode)

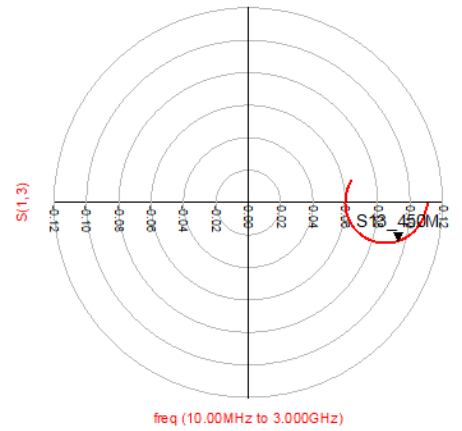
Condition : $V_{DD}=3.3V$, $V_{CTL}=1.8V$, $f=10$ to $3000MHz$, $T_a=+25^{\circ}C$, $Z_s=Z_L=50\Omega$



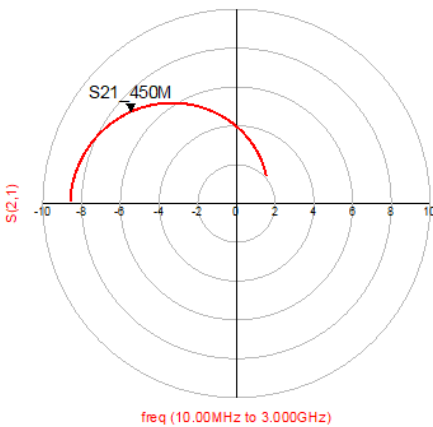
S11



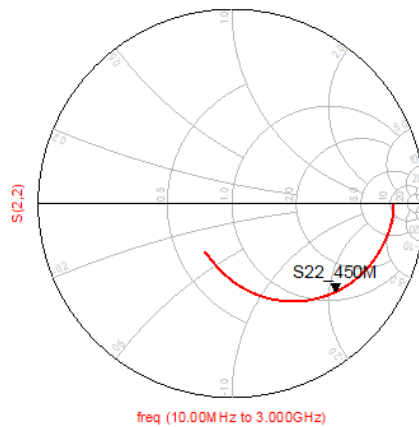
S12



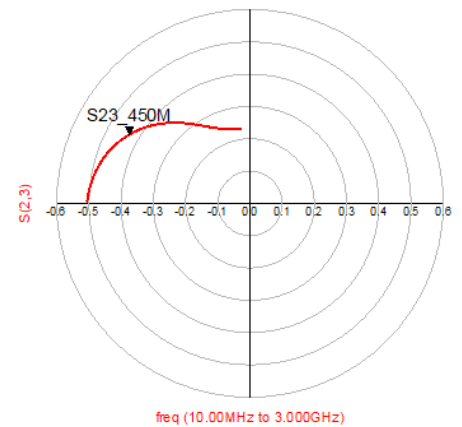
S13



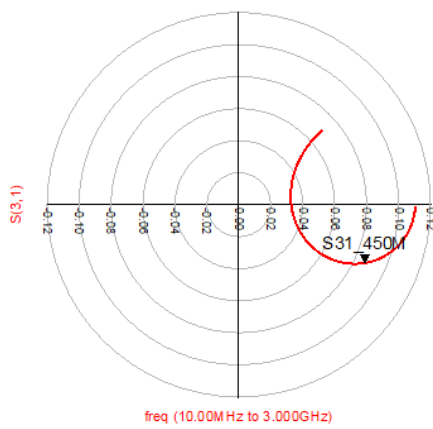
S21



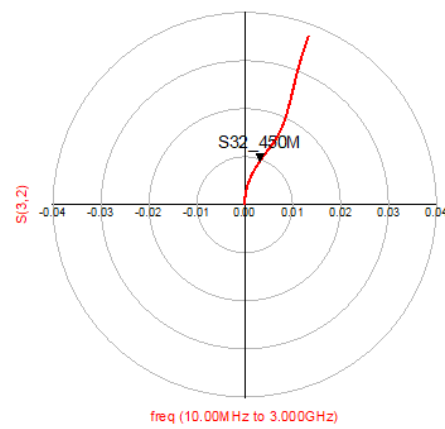
S22



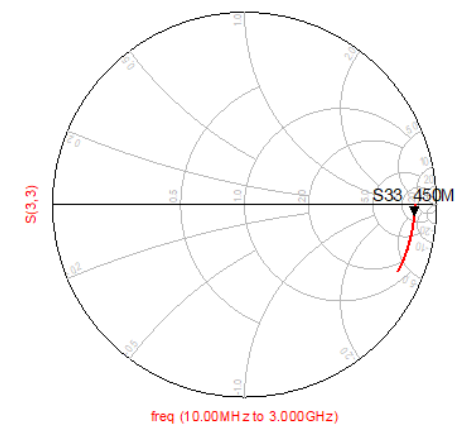
S23



S31



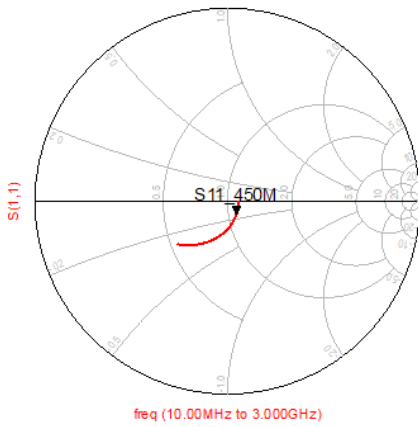
S32



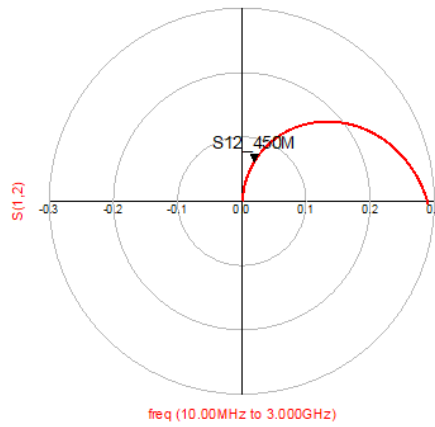
S33

■ S-parameter Simulation Data (Bypass mode)

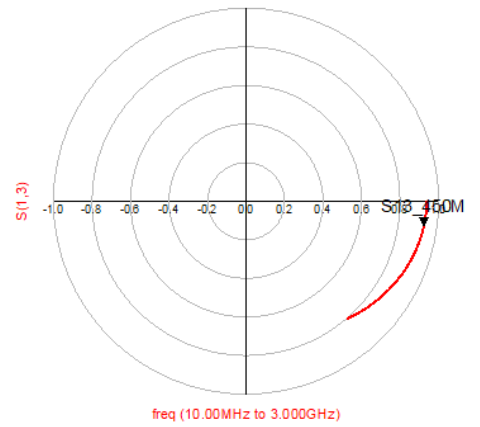
Condition: $V_{DD}=3.3V$, $V_{CTL}=0V$, $f=10$ to $3000MHz$, $T_a=+25^{\circ}C$, $Z_s=Z_l=50\Omega$



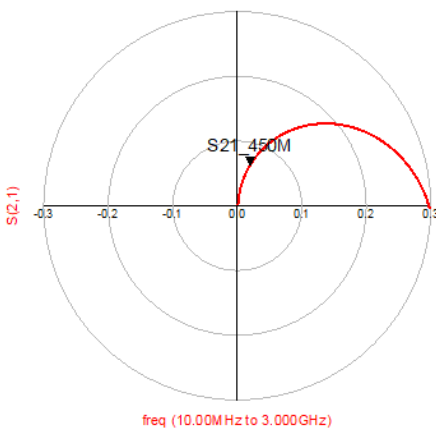
S11



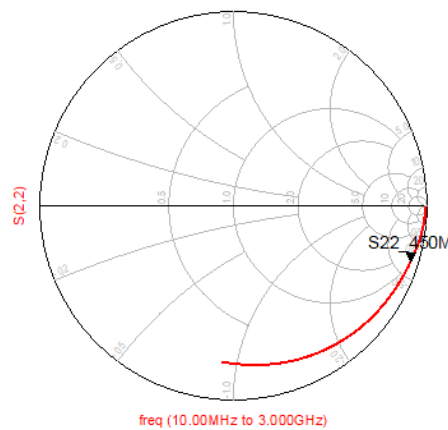
S12



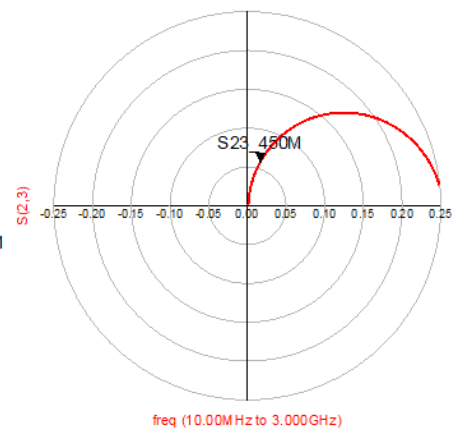
S13



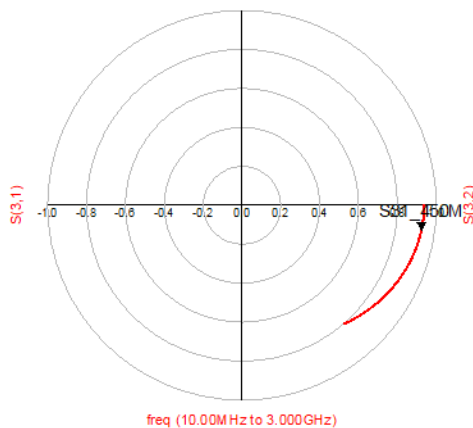
S21



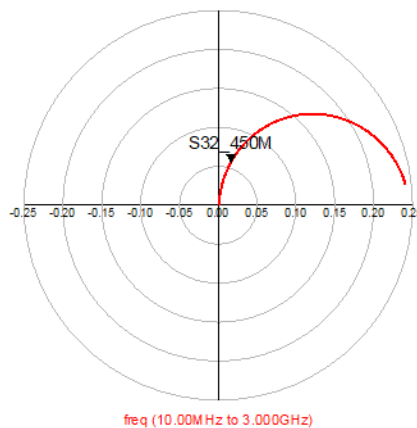
S22



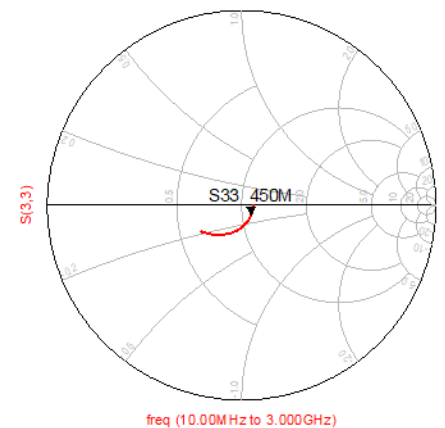
S23



S31



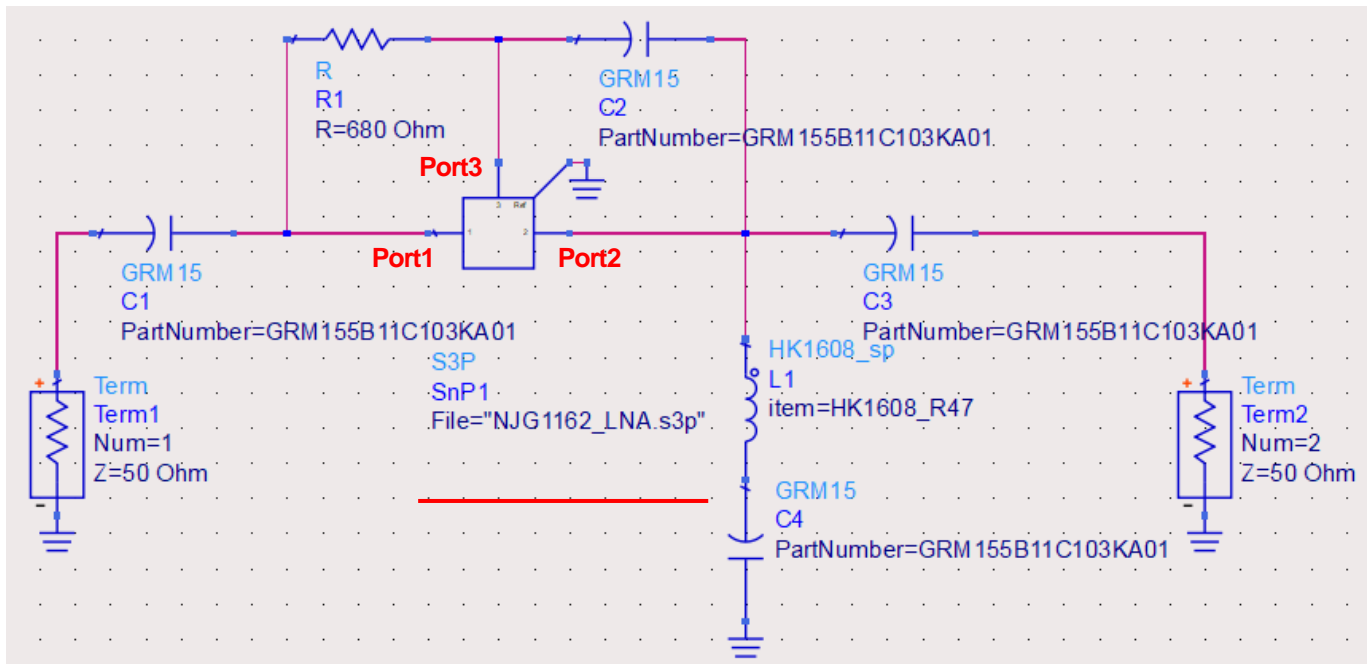
S32



S33



■ Simulation Example



Touchstone file : NJG1162_LNA.s3p (LNA mode)

f=10 to 1000MHz

