

Device Modeling Report

COMPONENTS : JFET OPERATIONAL AMPLIFIER

PART NUMBER : MUSES8920

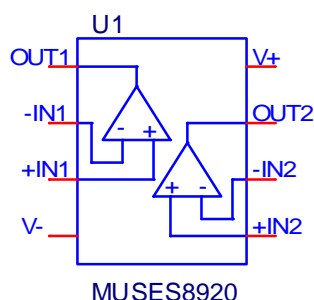
MANUFACTURER : NEW JAPAN RADIO CO.,LTD

Version : 2



新日本無線株式會社

Spice Model



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*$↓
*PART NUMBER:MUSES8920↓
*JFET OPAMP↓
*Version:2↓
*Please note that the inaccuracy is involved to it when you use this model.↓
*Please refrain from the model's resale.↓
*****↓
*Model Generated by NEW JAPAN RADIO CO.,LTD*↓
*      All Rights Reserved      *↓
*  Commercial Use or Resale Restricted  *↓
*****↓
.subckt MUSES8920 OUT1 -IN1 +IN1 V- +IN2 -IN2 OUT2 V+↓
X1_U1 +IN1 -IN1 V+ V- OUT1 MUSES8920_s↓
X2_U2 +IN2 -IN2 V+ V- OUT2 MUSES8920_s↓
.ends MUSES8920↓
*$↓
* connections:
*
*      non-inverting input↓
*      | inverting input↓
*      | positive power supply↓
*      | negative power supply↓
*      | output↓
*      |
*      1 2 3 4 5↓
.subckt MUSES8920_s 1 2 3 4 5↓
C1 11 12 {C1}↓
C2 15 16 {C2}↓
CS 10 0 {CS}↓
D1 16 17 DMOD1↓
D2 17 16 DMOD1↓
D3 5 18 DMOD2↓
D4 19 5 DMOD2↓
D5 10 20 DMOD2↓
VTL 3 20 {VTL}↓
GB 16 0 15 0 {GB}↓
GA 15 0 11 12 {GA}↓
GC 0 17 5 0 {GC}↓
GCM 0 15 10 0 {GCM}↓
ITL 3 10 {ITL}↓
M1 11 2 13 13 PMOS1 ↓
M2 12 NET1 14 14 PMOS2 ↓
RO1 16 5 {RO1}↓
RC 17 0 {RC}↓
RO2 16 0 {RO2}↓
R2 15 0 10QE3↓

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RD1 11 21 {RD1}↓
RD2 12 22 {RD2}↓
VRD1 21 4 {VRD}↓
VRD2 22 4 {VRD}↓
RS2 10 14 {RS2}↓
RS1 10 13 {RS1}↓
IDS 3 4 {IDS}↓
RP 3 4 {RP}↓
Vos 1 NET1 DC {VOS}↓
VS 19 4 DC {VS}↓
VD 3 18 DC {VD}↓
.MODEL DMOD1 D(T_MEASURED= 25 IS= 1.57E-63)↓
.MODEL DMOD2 D(T_MEASURED= 25 IS= 8.00E-16)↓
.MODEL PMOS1 PMOS(LEVEL=1 VTO= -4.89E-01↓
+ KP= 4.01E-05 L={L_VAL} W={W_VAL} TOX= 1.30E-08 U0= 1.51E+02)↓
.MODEL PMOS2 PMOS(LEVEL=1 VTO= -4.89E-01↓
+ KP= 4.01E-05 L={L_VAL} W={W_VAL} TOX= 1.30E-08 U0= 1.51E+02)↓
*↓
.PARAM↓
+ C1 = 1.09E-13↓
+ C2 = 5.3E-11↓
+ CS = 0.00E+00↓
+ GCM = 1.31E-08↓
+ GA = 4.15E-03↓
+ GB = 430.86↓
+ GC = 1615723.038↓
+ ITL = 1.50E-03↓
+ RD1 = 241.14↓
+ RD2 = 241.14↓
+ RC = 6.19E-07↓
+ RS1 = 26.20↓
+ RS2 = 26.20↓
+ RO1 = 50↓
+ RO2 = 25↓
+ RP = 2.40E+04↓
+ VD = 2.028230866↓
+ VS = 2.028230866↓
+ VOS = 7.97377E-04↓
+ IDS = 6.7E-3↓
+ VTL = 9.09E-01↓
+ VRD = 1.45E+00↓
+ L_VAL= 1.00E-05↓
+ W_VAL= 3.60E-03↓
.ends MUES8920_s↓
*$↓

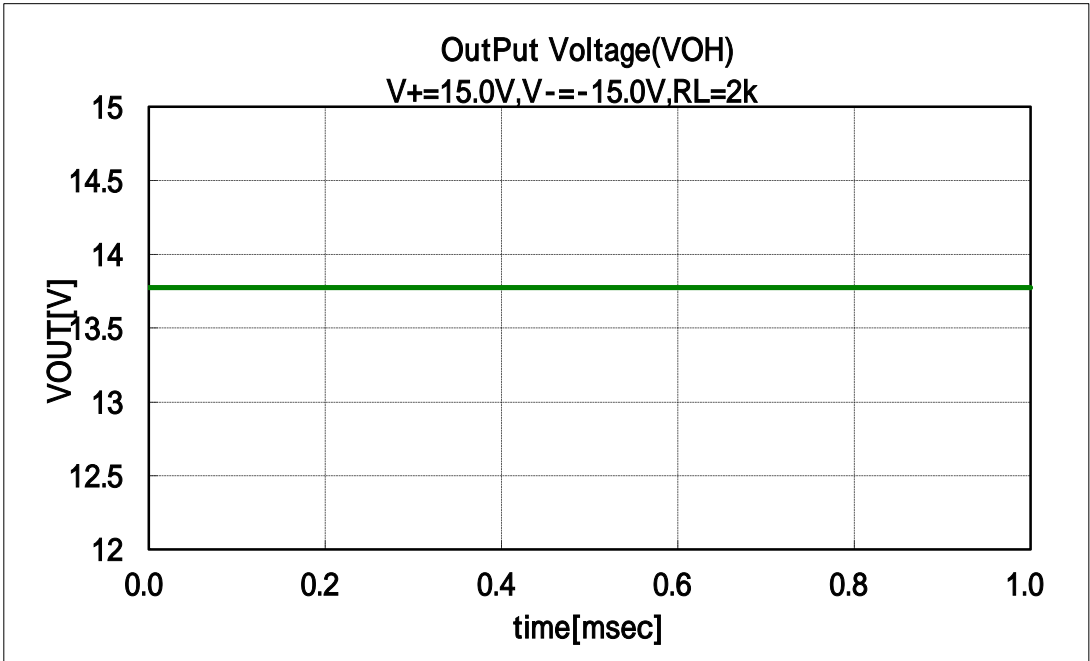
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MOSFET MODEL

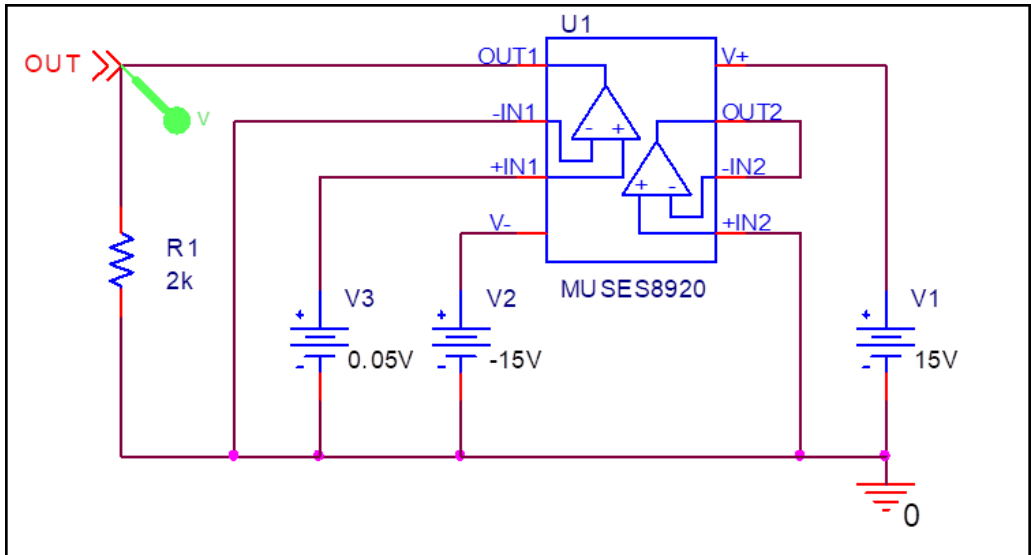
Pspice model parameter	Model description
T_MEASURED	Measured temperature
IS	Bulk Junction Saturation Current
VTO	Zero-bias Threshold Voltage
KP	Transconductance
L	Channel Length
W	Channel Width
TOX	Gate Oxide Thickness
U0	Surface Mobility

Output Voltage Swing (VOH)

Simulation result



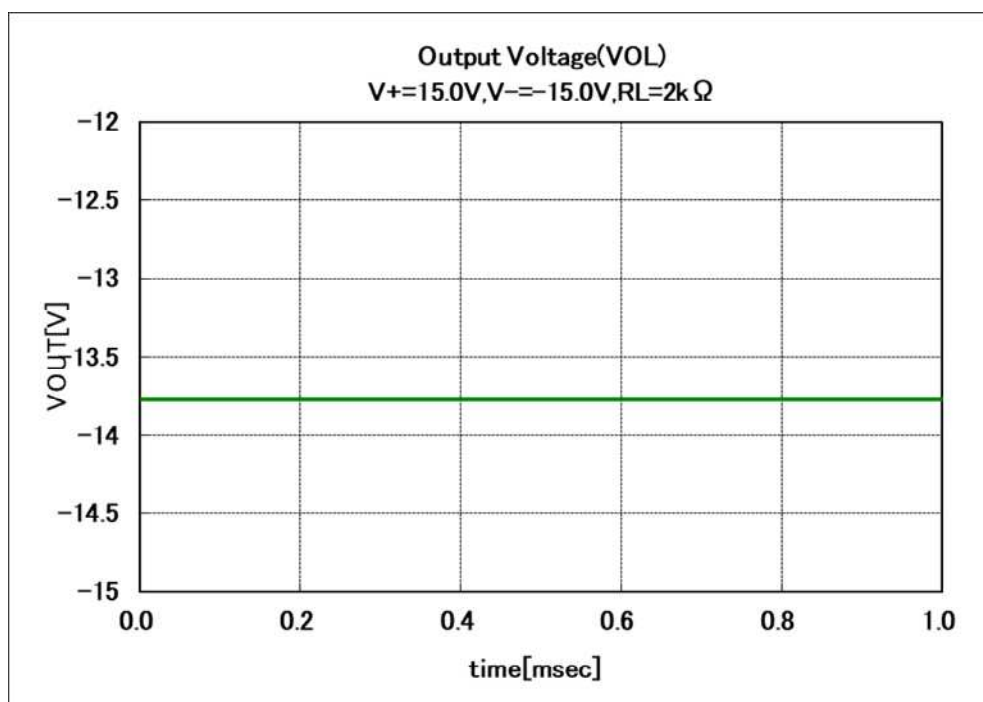
Evaluation circuit



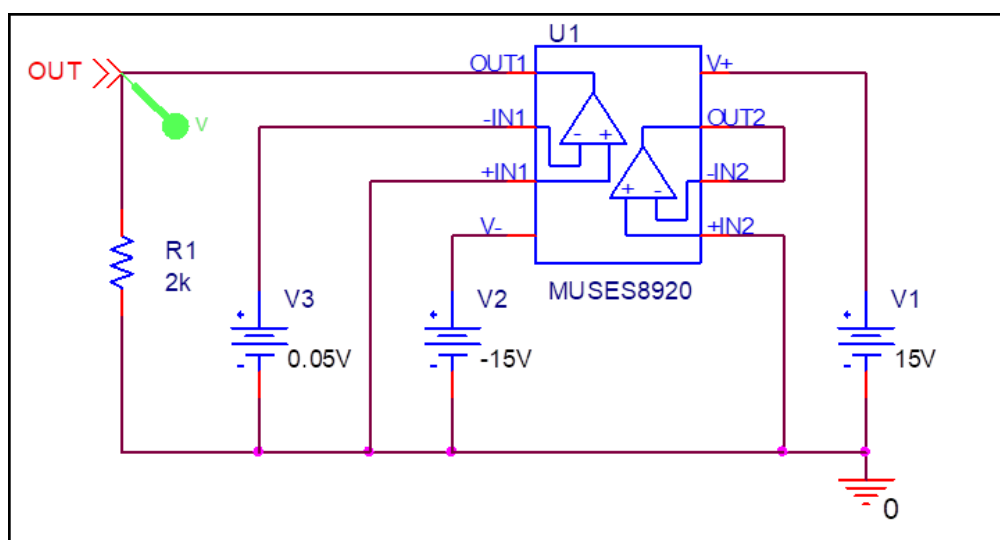
VOH(V)	Data sheet	Simulation	%Error
	13.8	13.8	0.0

Output Voltage Swing (VOL)

Simulation result



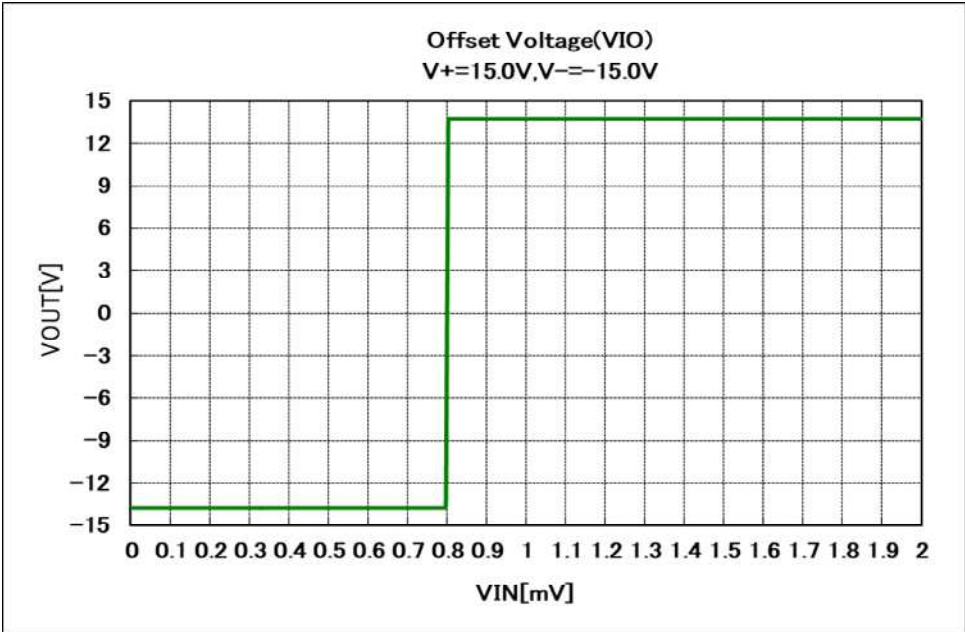
Evaluation circuit



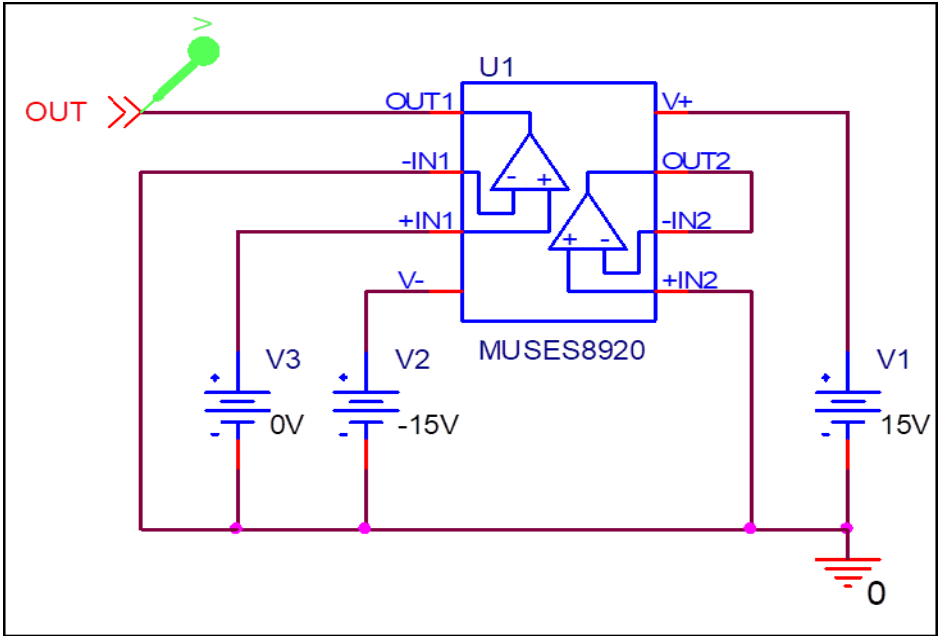
VOL(V)	Data sheet	Simulation	%Error
	-13.8	-13.8	0.0

Input Offset Voltage(VIO)

Simulation result



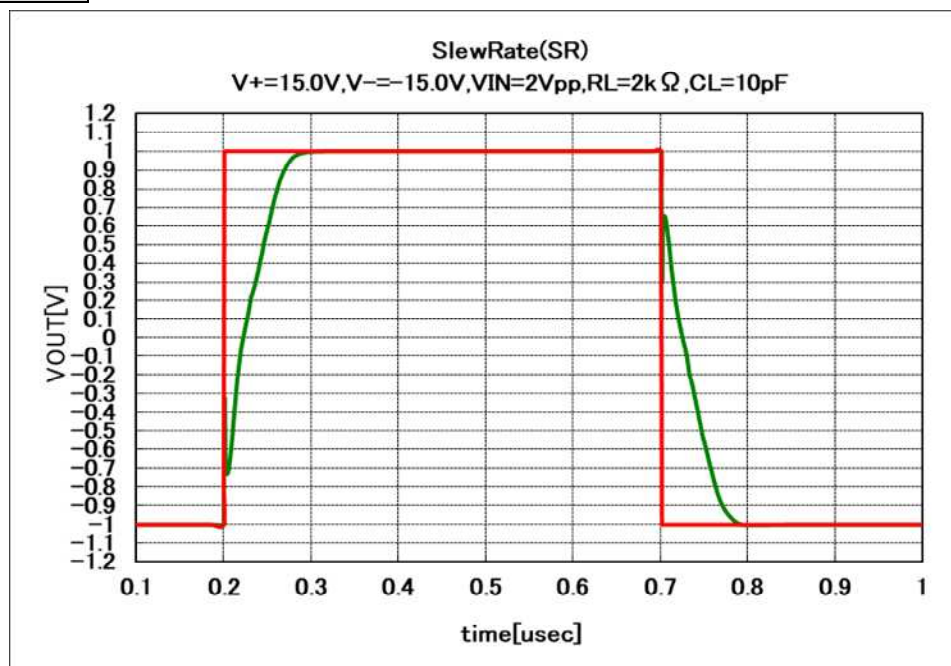
Evaluation circuit



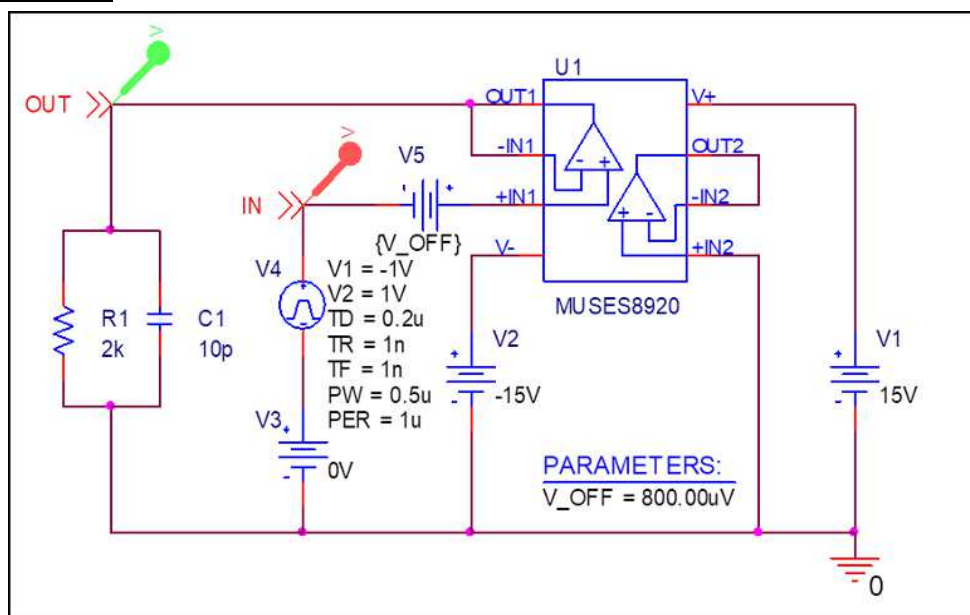
VIO(uV)	Measurement	Simulation	%Error
	800	800	0.0

Slew Rate (+SR, -SR)

Simulation result



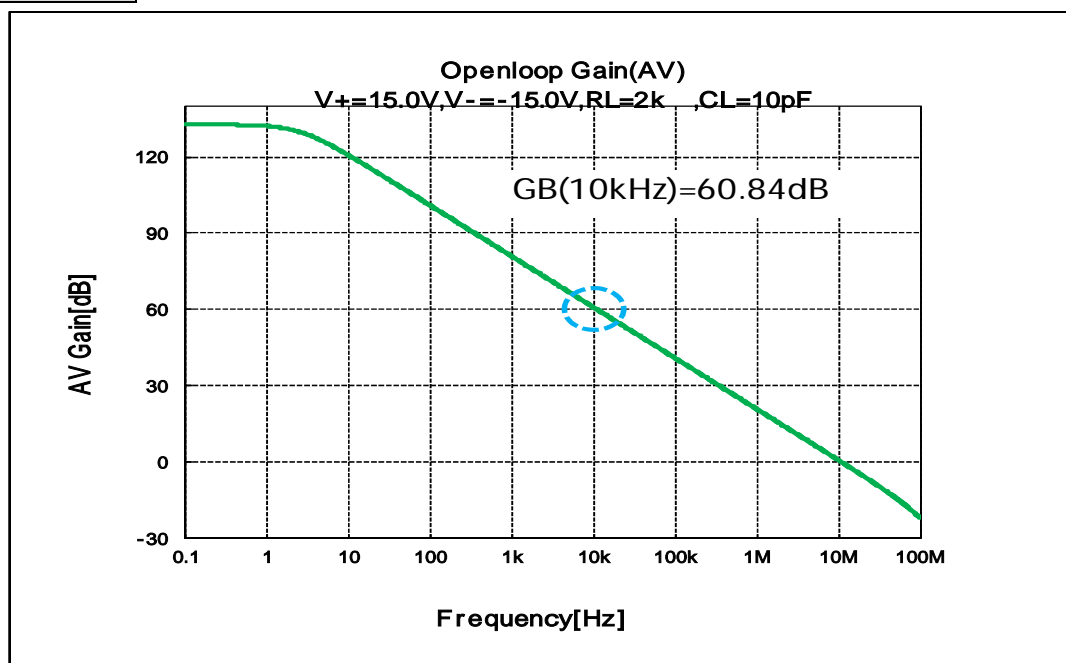
Evaluation circuit



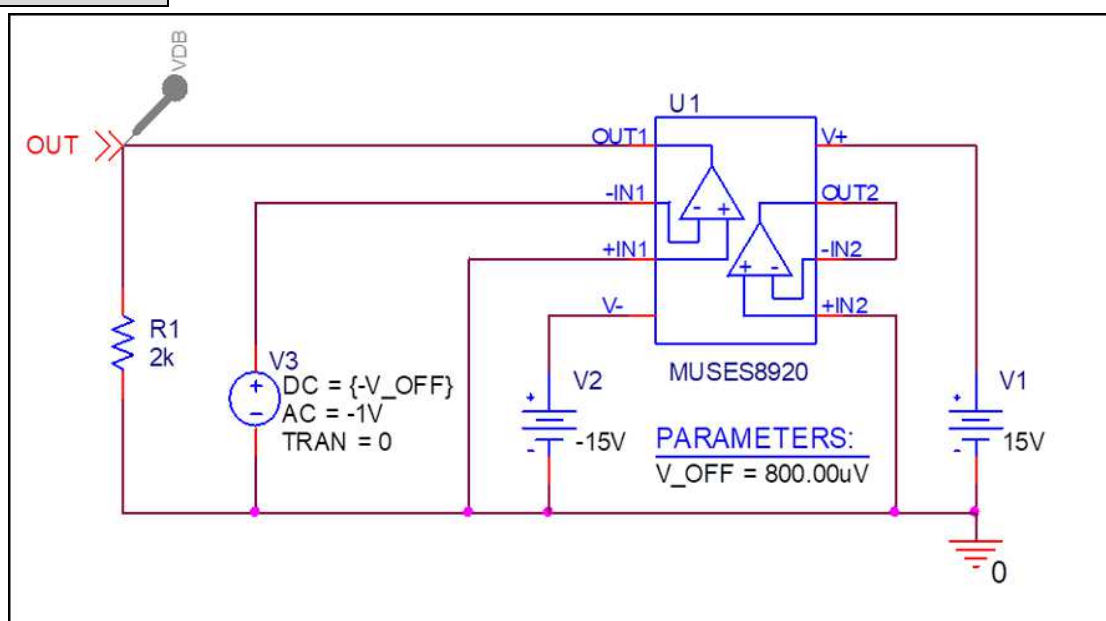
Slew Rate	Data sheet	Simulation	%Error
SR(V/usec)	25	26.76	7.04
-SR(V/usec)	-25	-24.13	3.48

Open Loop Voltage Gain (AV)

Simulation result



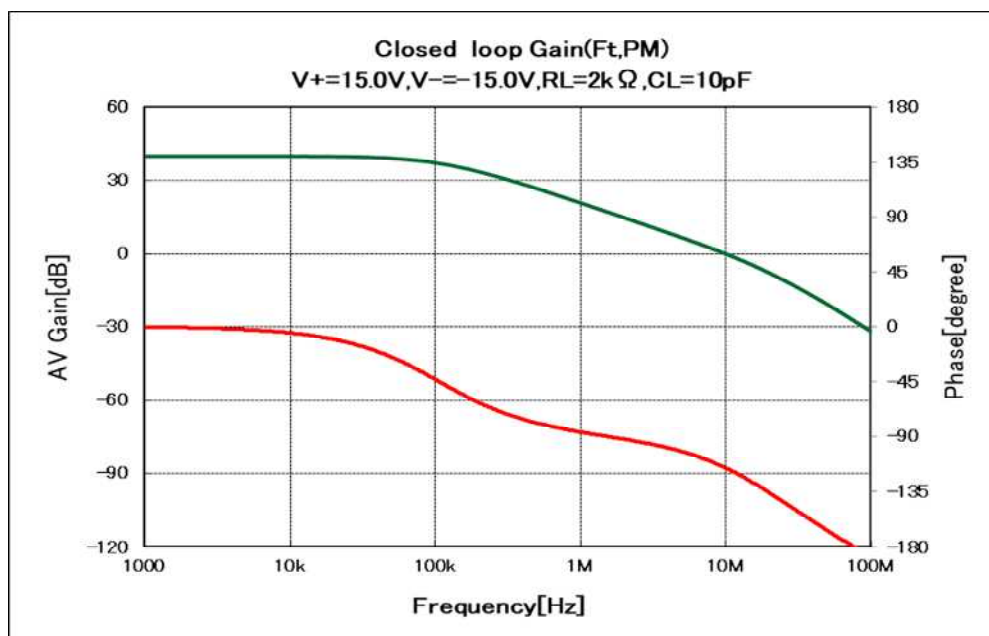
Evaluation circuit



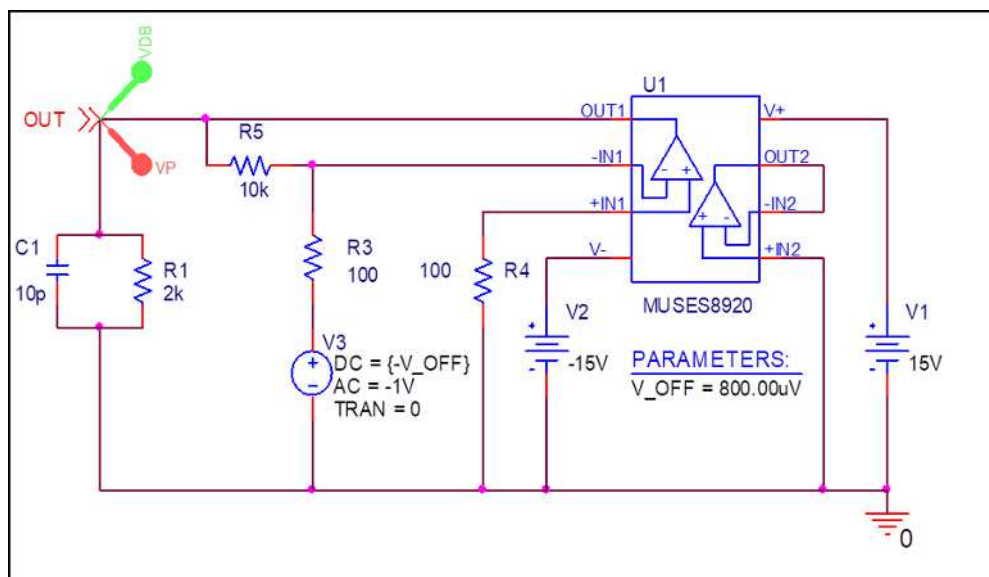
	Data sheet	Simulation	%Error
Av (dB)	133	132.68	0.24
GBW(MHz)	11	11.0	0.0

Closed Loop Voltage Gain (AV)

Simulation result



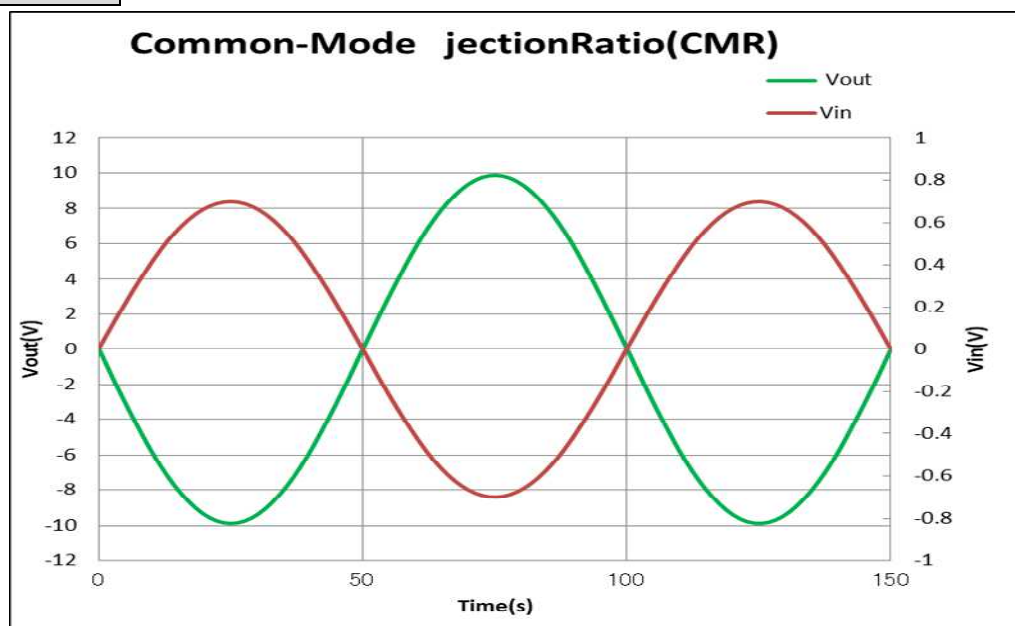
Evaluation circuit



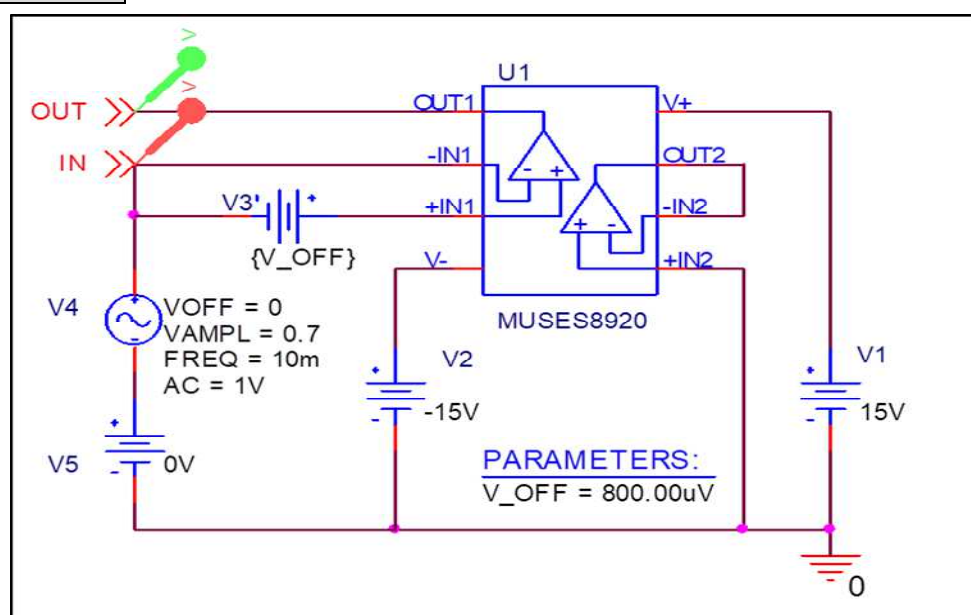
	Data sheet	Simulation	%Error
Ft(MHz)	10	9.89	1.1
m (Deg)	70	64	8.6

Common-Mode Rejection Voltage gain

Simulation result



Evaluation circuit



CMR(dB)	Data sheet	Simulation	%Error
	110	109.69	0.28