

February 4, 2022

NJG1801K75
SPDT Switch

S Parameter Simulation Data
0.1GHz to 8.5GHz

Ver.1

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■ **SIMULATION CONDITION**

$f=0.1\text{GHz to }8.5\text{GHz}$, Step=10MHz

VCTL=0/3.0V

$T_a=25^{\circ}\text{C}$,

$Z_i=Z_o=50\Omega$

DC blocking capacitors are connected to P1, P2, and PC ports.

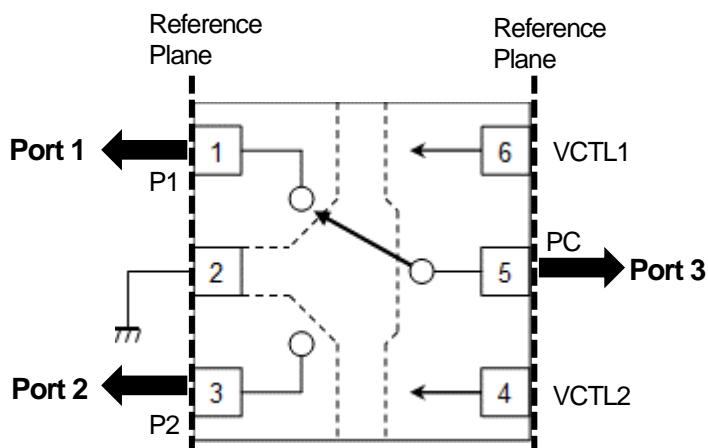
■ **DATA**

Touchstone (s3p)

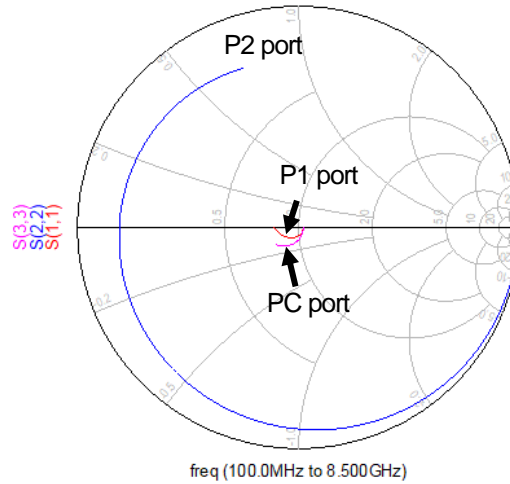
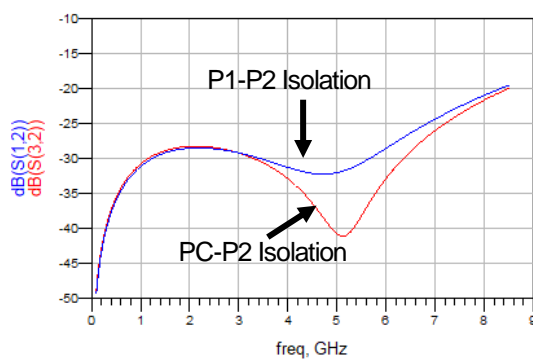
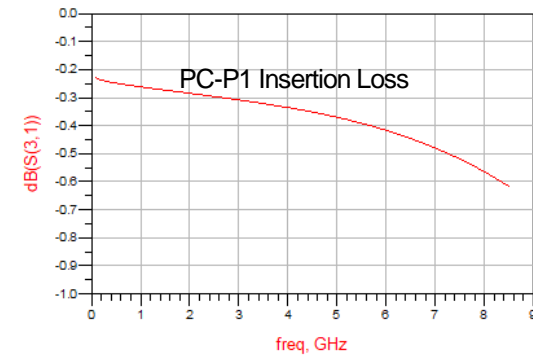
No.	Path	File name
1	PC-P1	NJG1801K75_P1on_8R5GHz.s3p
2	PC-P2	NJG1801K75_P2on_8R5GHz.s3p

■ **PORT DEFINITION**

Port No.	Terminal
1	P1 terminal
2	P2 terminal
3	PC terminal



File name: NJG1801K75_P1on_8R5GHz.s3p (PC-P1 ON mode)



File name: NJG1801K75_P2on_8R5GHz.s3p (PC-P2 ON mode)

